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# A fast channel simulation framework based on hierarchical waveform representations

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**Abstract**—We present a modeling framework for high-speed coupled channels, which allows for the simulation of millions of bits in few seconds. The modeling approach extends the standard IBIS-AMI by including common-mode signals. Further, an expansion of the transient responses at both driver and receiver ports into hierarchical basis functions allows to easily represent long-term memory effects due to the possibly slow dynamics of pre-emphasis blocks. Numerical experiments demonstrate the high accuracy and efficiency of the proposed technique.

## I. INTRODUCTION

The objective of this work is to present a novel high-speed serial link simulation method, whose objective is the evaluation of the transient waveforms at the receiver input due to switching signals comprising millions of bits, in just few seconds. This task is nowadays considered as a commodity in modern commercial channel simulation tools adopting the IBIS-AMI standard. This work wants to overcome some of the limitations of the latter approach.

First, we treat the general case of multiport transceivers connected by coupled channels, allowing for a seamless modeling and simulation of both differential and common-mode waveforms. Second, we propose a novel expansion of the transient responses in terms of a hierarchical set of multilevel transient basis functions. This expansion is motivated by the special form that the pre-emphasis circuitry embedded in the driver induces in the transient responses, which may present long-term memory effects due to the slow dynamics of the corresponding digital filter blocks. These effects may induce a different shape in the elementary waveforms accounting for elementary switching, depending on how many successive switching events precede each transmitted bit. This phenomenon may be hard to model within the IBIS-AMI framework, which is based on weighted precursors and postcursors that are just rescaled versions of the same elementary pulse. The proposed signal representation overcomes this limitation through successive hierarchical refinements that converge to the reference responses.

The proposed formulation is based on linearity assumptions, so that superposition holds. This enables frequency-domain (FFT) or time-domain (recursive convolution) approaches to compute transient responses. We adopt the former frequency-domain approach, which naturally plugs into the existing IBIS-AMI framework by suitably extending its scope and applicability.

## II. MODELING MULTIPORT TRANSCIEVERS

For the sake of illustration and without loss of generality, the following discussion is entirely based on differential drivers, since receivers can be seen as a simpler particular case. With reference to Fig. 1, we propose the following model structure

$$\mathbf{i}(t) = \mathbf{G}\mathbf{v}(t) + \mathbf{j}(t) + \mathbf{g}(\mathbf{v}(t)) \quad (1)$$

where  $\mathbf{i} = [i_1, i_2]^T$  and  $\mathbf{v} = [v_1, v_2]^T$  are the (single-ended) port variables<sup>1</sup>. The (constant) conductance matrix  $\mathbf{G}$  and the dynamical (LTI, Linear Time-Invariant) submodel  $\mathbf{g}$  account for the static and the dynamic behavior of the port currents, respectively. The time-varying source term  $\mathbf{j}(t) = [j_1(t), j_2(t)]^T$  represents the switching activity of the driver (voltage  $v_{in}(t)$  in Fig. 1) as a time-varying analog waveform.

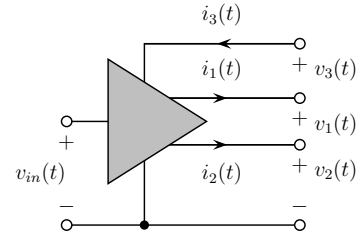


Fig. 1. Typical structure of a differential driver with its relevant port variables.

The above structure can be seen as a particular case of both state-of-the-art two-piece modeling formats known as IBIS and Mpiilog [1], [4]. In fact, the latter Mpiilog structure reads

$$\mathbf{i}(t) = \mathbf{w}_H(t)\mathbf{F}_H(\mathbf{v}(t)) + \mathbf{w}_L(t)\mathbf{F}_L(\mathbf{v}(t)) \quad (2)$$

where  $\mathbf{F}_\nu$  with  $\nu \in \{H, L\}$  are nonlinear dynamical multivariate relations accounting for the static and the dynamic behavior of the driver in fixed logic states, and  $\mathbf{w}_\nu$  are time varying switching functions. A similar structure holds for IBIS [1]. The proposed model structure (1) is easily derived from (2) under the following assumptions:

- symmetrical switching weights,  $\mathbf{w}_H(t) = 1 - \mathbf{w}_L(t)$ ;
- submodels  $\mathbf{F}_\nu$  approximated as LTI blocks

$$\mathbf{F}_\nu(\mathbf{v}) = \mathbf{G}_\nu\mathbf{v} + \mathbf{I}_\nu + \mathbf{g}_\nu(\mathbf{v}), \quad \nu \in \{H, L\} \quad (3)$$

<sup>1</sup>We adopt a voltage-current representation for simplicity, although other port representations are possible. Indeed, in our implementation we adopt a scattering (voltage) wave formulation for enhanced numerical stability.

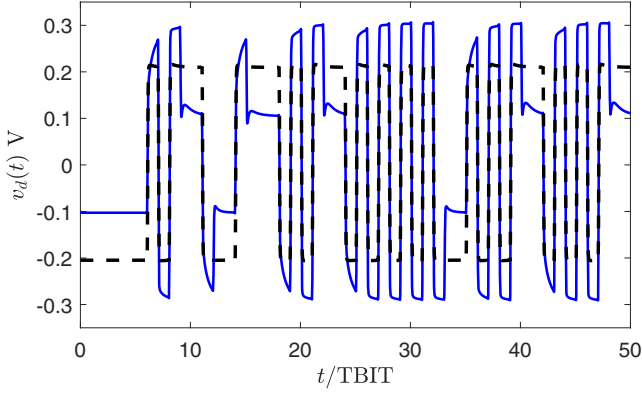


Fig. 2. Switching pattern of  $v_d(t) = v_1(t) - v_2(t)$  with (blue) and without (black) pre-emphasis for the example driver.

including both a linear multivariate static characteristic (defined by conductance matrices  $\mathbf{G}_\nu$  and static bias current vectors  $\mathbf{I}_\nu$ ), and a dynamic LTI submodel  $\mathbf{g}_\nu$  which approximates the device behavior in each fixed logic state;

- the driver is symmetric in both its static part  $\mathbf{G}_H = \mathbf{G}_L = \mathbf{G}$  and its dynamic part  $\mathbf{g}_H = \mathbf{g}_L = \mathbf{g}$ .

The various parameters of the model are estimated from a set of Transistor-Level (TL) simulations [4]. First, the static multivariate characteristics  $\mathbf{F}_\nu$  are extracted by a set of double DC sweeps, and the best linear approximations are obtained by a least-squares fit obtaining  $\mathbf{G}_\nu$  and  $\mathbf{I}_\nu$ . Second, the dynamic submodels  $\mathbf{g}_\nu$  are obtained through Time-Domain Vector Fitting [5] applied to port waveforms obtained through TL transient simulations. Finally, the switching sources  $\mathbf{j}(t)$  are extracted from the computed current and voltage responses of the driver switching on a given load. The switching term  $\mathbf{j}(t)$  plays in our framework the same role of the weighting functions  $\mathbf{w}_\nu(t)$  in standard IBIS/Mpilog models, providing in particular an effective behavioral representation of the driver pre-emphasis blocks.

### III. MODELING LONG-TERM MEMORY EFFECTS OF PRE-EMPHASIS BLOCKS

The main motivation for the proposed approach is best appreciated from Fig. 2, where the switching patterns of a commercial 40-nm low-power driver (available as a transistor-level encrypted netlist), with and without its (1-tap) pre-emphasis activated. As expected, pre-emphasis boosts switching events. It can be noted that the maximum peak-to-peak amplitude of the waveforms is obtained after a few successive switchings, with a slow dynamic saturation effect. This effect makes each individual switching front different from each other, based on the number of preceding consecutive switching events. Therefore, standard translation-invariant approaches that construct transient waveforms and eye diagrams through superposition of the same elementary pulse centered at multiple UIs do not seem to be adequate, since the shape of the switching fronts is not translation-invariant.

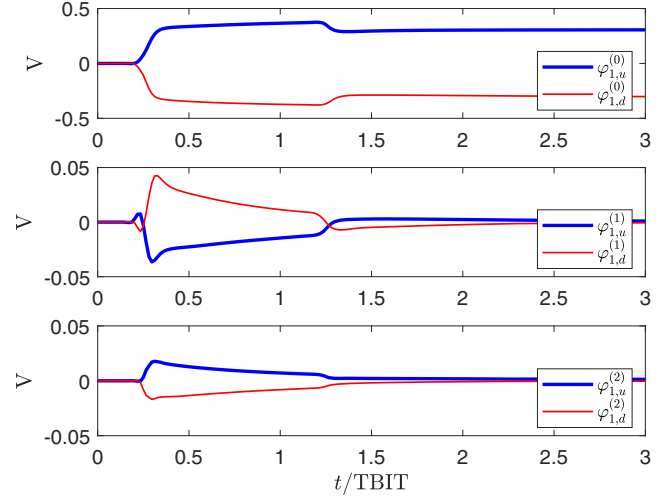


Fig. 3. Basis functions  $\varphi_{n,u}^{(\ell)}(t)$  and  $\varphi_{n,d}^{(\ell)}(t)$ , for  $n = 1$  and  $\ell = \{0, 1, 2\}$ .

Our solution to accurately represent switching fronts that are bit-pattern-dependent involves expansion of the driver source terms  $\xi_n(t) = j_n(t) - j_n(0)$  as the following sparse hierarchical superposition

$$\xi_n(t) = \sum_{\ell=0}^L \left[ \sum_{k \in \Omega_{n,u}^{(\ell)}} \varphi_{n,u}^{(\ell)}(t - kT_B) + \sum_{k \in \Omega_{n,d}^{(\ell)}} \varphi_{n,d}^{(\ell)}(t - kT_B) \right] \quad (4)$$

where  $n = 1, 2$  are the components of the source vector in (1),  $T_B$  is the bit time (UI),  $u, d$  denote, respectively, '01' and '10' transitions, and  $L$  is the maximum number of hierarchical levels (usually 3-4 levels are sufficient). At each level  $\ell$ , the index sets  $\Omega_{n,\nu}^{(\ell)}$  locate the switching events of type  $\nu = \{u, d\}$  that are immediately followed by at least  $\ell$  consecutive switchings. The corresponding basis functions  $\varphi_{n,\nu}^{(\ell)}(t)$  at each level  $\ell$  characterize the incremental correction that must be applied to the waveform accounting for all lower levels up to  $\ell - 1$  in order to account for the difference in switching behavior due to the presence of the additional consecutive  $\ell$ -th switching. The amplitude of such basis functions decreases with  $\ell$ , as depicted in Fig. 3.

For any realistic switching pattern, the size of the index sets  $\Omega_{n,\nu}^{(\ell)}$  decreases when increasing  $\ell$ , since the probability of occurrence of consecutive  $\ell$  switching events decreases. Note that these index sets are determined by a digital preprocessing of the logic bit sequence and they are exact. The basis functions  $\varphi_{n,\nu}^{(\ell)}(t)$  are estimated from training signals designed to include all combinations of the required switching patterns. Isolated switchings are processed first to derive  $\varphi_{n,\nu}^{(0)}(t)$ . The corresponding approximate signals are reconstructed, subtracted from the training signals, and double switching events are processed to extract  $\varphi_{n,\nu}^{(1)}(t)$ . The procedure is then iterated until all required levels have been extracted.

### IV. COMPLETE CHANNEL SIMULATION AND RESULTS

Consider now the simulation of a coupled channel terminated by differential (multiport) driver and receiver modeled

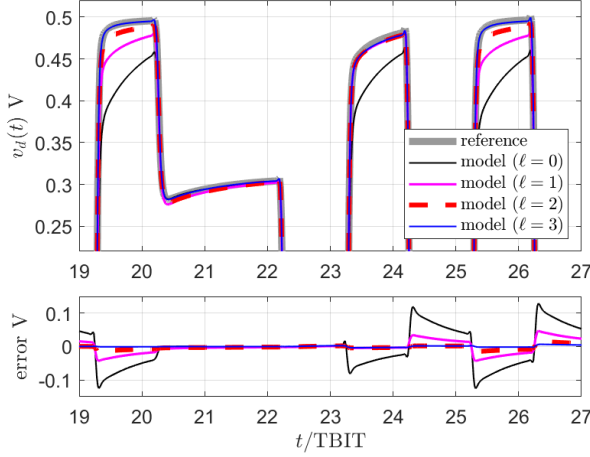


Fig. 4. Received voltages computed through superposition of increasing hierarchical levels (top) and error (bottom).

as discussed above (the receiver is modeled as the driver but removing the time-varying sources). Due to the linearity of all submodels, the global transfer functions between the source terms  $\xi_n(t)$  and the desired output (voltage) waveform  $\eta_m(t) = v_m(t) - v_m(0)$  can be obtained in frequency domain as  $H_{mn}(j\omega)$ . The latter is obtained by suitably cascading driver, channel and receiver frequency responses. A standard FFT processing is then applied to compute the transient responses at the receiver due to the individual basis functions  $\varphi_{n,u}^{(\ell)}(t)$  and  $\varphi_{n,d}^{(\ell)}(t)$ . We denote these responses as  $\psi_{mn,u}^{(\ell)}(t)$  and  $\psi_{mn,d}^{(\ell)}(t)$ , which in turn are used to express the received voltages as

$$\eta_{mn}(t) = \sum_{\ell=0}^L \left[ \sum_{k \in \Omega_{n,u}^{(\ell)}} \psi_{mn,u}^{(\ell)}(t - kT_B) + \sum_{k \in \Omega_{n,d}^{(\ell)}} \psi_{mn,d}^{(\ell)}(t - kT_B) \right] \quad (5)$$

This expression is identical to (4) but uses different (known) basis functions. In particular, it inherits sparsity due to the hierarchical multilevel expansion.

Figure 4 shows the received voltages at the end of a coupled lossy channel driven by the driver of Fig. 2 with pre-emphasis enabled, obtained by successive superposition of increasing levels. It is noted that when only level  $\ell = 0$  is included, only isolated switching events are correctly represented. Including also level  $\ell = 1$  provides an accurate representation of any pair of bits that are consecutively switching. Adding more levels leads to convergence for all possible switching sequences.

The received waveforms (5) are readily converted into eye diagrams. Thanks to linearity, common approaches for inclusion of deterministic and random jitter, as well as crosstalk, can be used in a post-processing phase, as in standard IBIS-AMI flows. An example (including jitter and crosstalk) is reported in Fig. 5. This example was obtained by processing a PRBS-31 pattern of one million bits. Our prototypal non-optimized MATLAB implementation returned this result in 29

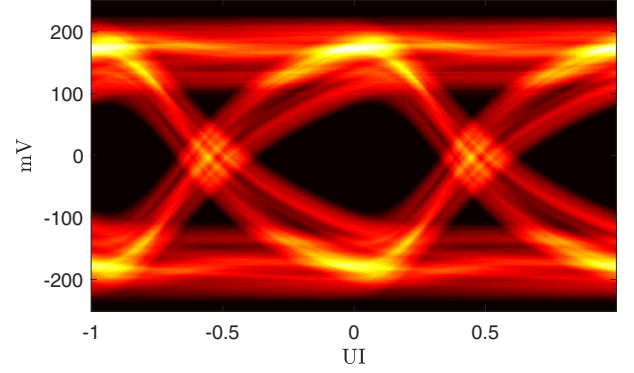


Fig. 5. Eye diagram obtained by processing a  $10^6$  bit PRBS-31 pattern.

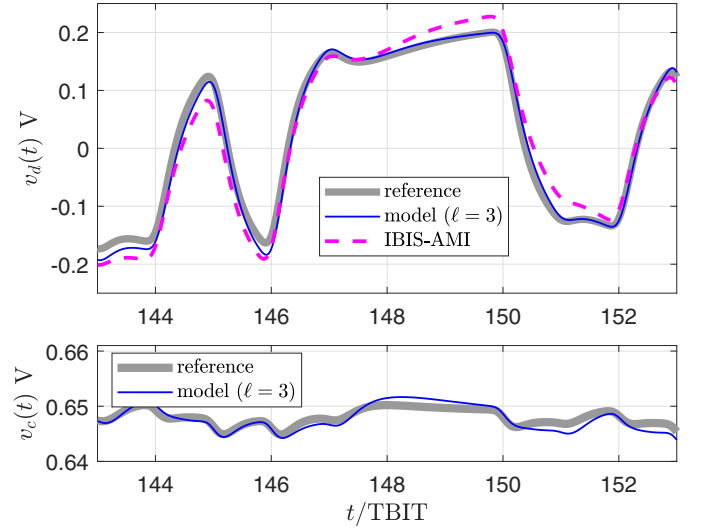


Fig. 6. Received differential (top) and common-mode (bottom) voltages, computed by different models.

seconds using a standard laptop (Intel Core i7-7500U CPU @ 2.70 GHz, 16.0 GB RAM).

The improvements that our approach may provide with respect to IBIS-AMI standard models are documented in Fig. 6, which compares the received voltage computed using the true TL model to the proposed solution and to the solution obtained by a standard IBIS-AMI model (for which there is no common-mode voltage prediction).

## REFERENCES

- [1] I/O Buffer Information Specification version 5.1, [Online] Available: <http://ibis.org/specs/>.
- [2] I. S. Stievano, I. A. Maio, and F. G. Canavero, "M $\pi$ log, macromodeling via parametric identification of logic gates," *IEEE Trans. Adv. Packag.*, vol. 27, no. 1, pp. 15-23, Feb. 2004.
- [3] G. Signorini, C. Siviero, M. Telescu, I.S. Stievano, "Present and Future of I/O-Buffer Behavioral Macromodels", *IEEE Electromagnetic Compatibility Magazine*, Vol. 5, No. 3, pp. 79-85, 2016.
- [4] G. Signorini, C. Siviero, S. Grivet Talocia, I.S. Stievano, "Macro-modeling of I/O Buffers via Compressed Tensor Representations and Rational Approximations", *IEEE Trans. Components, Packaging and Manufacturing Technology*, Vol. 6, No. 10, pp. 1522-1534, Oct. 2016.
- [5] S. Grivet-Talocia, "Package Macromodeling via Time-Domain Vector Fitting", *IEEE Microw. and Wireless Comp. Lett.*, Vol. 13, No. 11, pp. 472-474, Nov. 2003.